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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,589	10/17/2003	Sasson Somekh	004393 USA/02/MTCG/PCTRL/	7414

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EXAMINER	
FRANK, ELLIOT L	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,589	SOMEKH ET AL.	
	Examiner	Art Unit	
	Elliot L Frank	2125	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Four IDS in case*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The instant application is a continuation of application number 09/469,227 (patent 6,640,151 B1).

Double Patenting

2. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of Somekh et al. (USPN 6,640,151 B1). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

The claims of Somekh et al. patent contain every element of claim 1 of the instant application and as such anticipates claim 1 of the instant application. *In re Goodman*, 29 USPQ2d 2010 (CAFC 1993)

> "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus)." ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Specification

3. The abstract of the disclosure is objected to because it does not fully describe the invention and includes the purported merits of the invention. The abstract should be a 50-150 word narrative summary of the invention. Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities:

   a. Page 2, line 9 – The "station controllers" indicated in the specification as "(112-116)" should actually be "(106-110)" per the drawing figure.

   b. Appropriate correction is required.

Claim Objections

5. Claim 59 is objected to because of the following informalities:

   a. Claim contains the following phrase: "wherein said two more functional units use a unifying protocol, to thereby alleviate a need to use station controller for said two or more functional units."

   b. The examiner has only considered the "unifying protocol" as a limitation in this phrase. The rational for using the protocol is not deemed to further limit the claim because the motivation for using a "unifying protocol" does not physically alter the functioning of the claimed system.

   c. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-7,9-12 and 39-59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   a. Claim 1 recites the limitation "the individual tool" in line 1. There is insufficient antecedent basis for this limitation in the claim.

   b. Claims 1,5,9,39,43,54 and 59 and recite the limitation "the coordinated effort" in various lines within each claim's preamble. There is insufficient antecedent basis for this limitation in these claims.

   c. Claims 5 and 9 recite "A system for controlling the quality and/or quantity..." in line 1. There is no support in the claimed process for the output control of the quantity of a final semiconductor product. This limitation should be removed.

   d. The cited claims not specifically discussed above depend from a rejected claim and are rejected for containing the same deficiencies.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1,2,4-6,9,10,12,13,20-26,33-35,39-43,50-55,57 and 58 are rejected under 35 U.S.C. 102(e) as being anticipated by Breiner et al. (USPN 6,298,470 B1).

The limitations of the aforementioned claims, and the relevant citations in Breiner et al., are as follows:

1. A system for interactively monitoring and adjusting product output from the individual tool of a module, wherein the output is a result of the coordinated effort of two or more semiconductor preparation tools making up the module (column 2, lines 29-41), the system comprising;

a first tool of said two or more semiconductor tools, said first tool capable of implementing a first process on a semiconductor product and producing a first output;

a second tool of said two or more semiconductor tools, said second tool receiving as input said first output from said first tool, and said second tool capable of implementing a second process on the semiconductor product and producing a second output (column 5, line 39-column 6, line 8, wherein a multitude of process tools are controlled by the system).

wherein said first tool measures and obtains measurement data relating to the thickness and uniformity of a film, and wherein said measurement data is conveyed

to said second tool for use in modifying a behavior of said second tool (column 8, line 5-42); and

a module control mechanism, said module control mechanism capable of facilitating the exchange of information between said first tool and said second tool so that the module yields a desired semiconductor product output, said semiconductor product output being, or resulting from, said second output (column 5, line 39-column 6, line 8).

Claims 5 and 39 have the same functional limitations as claim 1, and are therefore anticipated by the same citations in Breiner et al.

2. The system of claim 1 wherein the said first tool includes a metrology station (column 5, line 39-column 6, line 8) and said second tool includes a chemical mechanical polishing apparatus (column 12, lines 8-25).

Claims 6 and 10 have the same functional limitations as claim 2, and are therefore anticipated by the same citations in Breiner et al.

4. The system of claim 1, wherein said module control mechanism is a part of said first tool, or is distributed between said first and second tools (column 3, lines 41-67).

Claims 12,22,23,34,35,41,42,52 and 53 have the same functional limitations as claim 4, and are therefore anticipated by the same citations in Bremer et al.

Claim 9 includes the same functional limitations as claim 1 with the additional requirement that the combined process yield a pre-set or user-specified result. This additional requirement is read in Bremer et al. at column 3, lines 25-40.

13. A system for interactively monitoring and adjusting product output from a module, wherein the output is a result of the coordinated effort of two or more semiconductor tools making up the module (column 2, lines 29-41), the system comprising:

a first tool of said two or more semiconductor tools, said first tool capable of implementing a first process on a semiconductor product and producing a first output (column 5, line 39-column 6, line 8);

a second tool of said two or more semiconductor tools, said second tool receiving as input said first output from said first tool, and said second tool capable of implementing a second process on the semiconductor product and producing a second output (column 8, lines 5-42, wherein a chain of processes receiving information from the previous process is described),

wherein one of said first or second tools measures and obtains measurement data relating to said semiconductor product, and wherein said measurement data is conveyed to the other of said first or second tools for use in modifying a behavior of said other of said first or second tool (column 6, line 44-column 7, line 14, wherein the feeding of information to various tools is described); and

a module communication mechanism, said module communication mechanism capable of facilitating the communication of information between said first tool and said second tool so that the module yields a desired semiconductor product,

said semiconductor product output being, or resulting from, said second output (column 5, line 39-column 6, line 8).

Claims 24,43 and 54 have the same functional limitations as claim 13, and are therefore anticipated by the same citations in Bremer et al.

20. The system of claim 13, wherein said measurement data relates to the thickness and/or uniformity of a film (column 4, lines 1-59).

Claims 25,50 and 55 have the same functional limitations as claim 20, and are therefore anticipated by the same citations in Bremer et al.

21. The system of claim 13, further comprising a module controller, wherein at least some information communicated by said module communication mechanism are controlled by said module controller (column 3, lines 41-67, wherein a myriad of different controller configurations are explained and examples are provided).

Claims 33,40 and 51 have the same functional limitations as claim 21, and are therefore anticipated by the same citations in Bremer et al.

26. The system of claim 24, further comprising a third functional unit, wherein the routing of a semiconductor product through said first, second and third functional units occurs in a pre-determined, fixed sequence (column 9, lines 38-49, Wherein a known process flow for semiconductor manufacturing is described).

Claims 57 and 58 require a system wherein said control is facilitated by the use of algorithmic instructions (column 3, lines 41-67).

Claims 1,2,4-6,9,10,12,13,20-26,33-35,39-43,50-55,57 and 58 are read in entirety in Breiner et al.

10. Claims 8 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Friedman (USPN 6,078,845 A).

The limitations of claims 8, and the applicable citations in Friedman are as follows:

8. A method for associating information with a wafer in a semiconductor processing facility (column 1, lines 5-10), comprising the steps of:

(1) processing a wafer at a first wafer processing tool, and storing first information pertaining to said wafer on a traveling information file, wherein said traveling information file comprises information pertaining to the status of said wafer (column 5, lines 21-27);

(2) transferring said wafer to a second wafer processing tool (Figure 1 and column 3, lines 34-51);

(3) transferring said traveling information file with said wafer to said second wafer processing tool;

(4) receipt of said traveling information file by said second wafer processing tool (steps 3 and 4 are read at column 6, lines 35-61); and

(5) processing said wafer at said second processing tool using said first information in said wafer status file, and storing second information pertaining to said wafer on said traveling information file (column 5, lines 4-20).

Claim 36 has the same functional limitations as claim 8, and therefore is anticipated by the same citations in the combined references.

Claims 8 and 36 are read in entirety in Friedman.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3,7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Breiner et al. (USPN 6,298,470 B1). In view of Bothra (USPN 5,916,016 A).

Claims 3,7 and 11 are dependent upon claims 1,5 and 9 respectively. Claims 1,5 and 9 have been shown to be anticipated by Breiner et al.

Breiner et al. does discuss the use of CMP with the processing system, however, it does not discuss using variable pressure regions when polishing a wafer.

Bothra, analogous to Breiner et al. in that both systems concern controlling semiconductor processing equipment, reads upon the additional requirements of claims 3,7 and 11 as follows:

3. The system of claim 2, wherein modifying the behavior of said second tool includes determining a plurality of pressures to apply to different regions of the semiconductor product as it is pressed against a polishing surface (column 2, line 52-column 3, line 3).

Claims 7 and 11 have the same functional requirements as claim 3, and therefore are obvious in view of the combined references.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the functionality of Bothra into Breiner et al. to obtain variably programmed back pressures during polishing operation which allows precision control of polishing rates over the surface of a wafer (Bothra, column 3, lines 4-9).

13. Claims 14-19, 27-32,44-49 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Breiner et al. (USPN 6,298,470 B1) in view of Dvir (USPN 6,212,961 B1).

Claims 14-19 depend from claim 1. Claim 1 is anticipated by Breiner et al.

Claims 14-19 describe different combinations of semiconductor processing equipment that are required as the first tool and second tool in the instant application. Breiner et al. makes obvious the use of these tools at column 3, lines 41-67, wherein a list of typical semiconductor processing tools is presented.

Claims 14-19 also require that the first tool obtains measurement data and passes it to the second tool. Where the first tool is not strictly a metrology tool, an integrated metrology tool would be required. While Breiner describes the use of in-situ metrology and monitoring tools (column 6, lines 15-32), it does not read specifically on whether they are integrated into the processing equipment.

Dvir, analogous to Breiner et al. in that both system deal with semiconductor processing control (Dvir, column 1, lines 11-13) is presented to demonstrate that integrated metrology tools were well known in the art at the time the invention was

made (column 1, lines 17-22). No motivation to combine has been presented since Dvir is only cited for demonstrating the state of the art when the invention was made.

Claims 27-32, 44-49 and 56 have functional requirements similar to claims 14-19 and are deemed obvious in view of the same citations in the combined references.

14. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friedman (USPN 6,078,845 A) in view of Stoddard et al. (USPN 6,587,744 B1).

Claims 37 and 38 have the same basic functional limitations as claim 8 with additional feedback and recipe requirements that are not specifically recited in Friedman.

Stoddard et al., analogous to Friedman in that both system concern semiconductor processing control (Stoddard et al., column 1, lines 15-18), reads on the additional requirements of Claim 37 and 38 as follows:

37. (7) processing a second wafer at said first wafer processing tool using said at least some of said second information of said step (6) (column 2, lines 17-41).

38. The method of claim 37, wherein wafer information entity contains a recipe or a modification of said recipe, and wherein said first wafer processing tool comprises the step of using said recipe or said modification of said recipe in said wafer information entity to process said wafer (column 4, lines 50-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the features of Stoddard et al. into the Friedman system have provided a system that could automatically make intelligent

decisions as to what variables to change in the recipe to maintain the desired process target (Stoddard et al., column 4, lines 50-59).

15. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Breiner et al. (USPN 6,298,470 B1) in view of Stoddard et al. (USPN 6,587,744 B1).

Claim 59 includes the same basic functional limitations as claim 5 with the additional requirement of using a unifying protocol not specifically read in Breiner et al.

Stoddard et al., analogous to Breiner et al. in that both system concern semiconductor processing control (Stoddard et al., column 1, lines 15-18), reads on the additional requirements of claim 59 at column 7, lines 48-65 and column 10, lines 30-47 wherein the use of a unifying protocol is recited.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the features of Stoddard et al. into the Breiner et al. system to have provided a user with a standardized means to acquire process data, as well as defining the format in which it is presented (Stoddard et al., column 7, lines 48-65).

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the

obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

USPN 5,838,951 A – Song – Metrology data transfer

USPN 6,427,093 B1 – Toprac – Semiconductor process control

USPN 6,580,958 B1 – Takano – Wafer tracking

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elliot L Frank whose telephone number is (703) 305-5442. The examiner can normally be reached on M-F 7-4:30, 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ELF
June 18, 2004

Albert W. Paladini 6-21-04

ALBERT W. PALADINI
PRIMARY EXAMINER